A1 Cont.

mask, the bit indicating whether the corresponding processor has not yet passed through a quiescent state.

REMARKS

Reconsideration of the application is respectfully requested. All claims were rejected under § 112, 2nd Paragraph and under § 103 as being unpatentable over Slingwine et. al. (U.S.P.N. 5,727,209) ("Slingwine") in view of Roche et. al., (U.S.P.N. 4,916,697) ("Roche"). An amendment to claim 1 is respectfully submitted relating solely to the § 112, 2nd Paragraph rejection. All rejections are traversed for the reasons given below.

Response to The Section 112, 2nd Paragraph Rejection

Claims 1-6 were rejected as incomplete for omitting essential elements. [Office Action, p. 2]. The Examiner referred to a gap between the elements, citing MPEP § 2172.01. However, MPEP § 2172.01, refers to two grounds of rejection, only one of which is a § 112, 2nd Paragraph, rejection: Failure "to interrelate essential elements of the invention as defined by applicant(s) in the specification." Applicant's response assumes this is the rejection made because it is the only § 112, 2nd Paragraph, rejection in MPEP § 2172.01. If the Examiner intended to reject under another statutory provision, it is respectfully requested that the office action be reissued under the correct statutory authority so that applicant may then respond. Applicant now respectfully responds to these rejections.

Claim 1: In response to the rejection, claim 1 is amended to use the complete term "physical memory" throughout rather than just "memory" in order to be consistent with the use of "physical memory" in the preamble. The claim language in the second paragraph of the claim is amended to clarify that the first level bit mask can be in any "physical memory accessible to all nodes." This amendment clarifies that the first level bit mask is not restricted to being in the physical memory of any particular node. It is logical that the first level bit mask be in memory accessible to all nodes because the bits of the first level bit mask contain information about nodes

as a group. Applicant believes that with this amendment the interrelationship between the memories in the claim and preamble is clear.

Also, the last paragraph of claim 1 is amended to make clearer that the bits in a second level bit mask contain information about processors associated with a particular node identified in the first level bit mask. The interrelationship between the first and second level bit masks is now set forth more clearly. The first level bit mask contains bits providing information about nodes. The second level bit masks contain bits providing information about processors associated with a particular node identified in the first level bitmask.

The Examiner found the relationship between the bit masks and the operation of the multi-processor system unclear and also found it unclear whether any processing is taking place. [Office Action, p. 3]. With the above amendments, applicant believes that both of these concerns are satisfactorily addressed. The interrelationship between the bit masks is clearer and that should also make their function relative to the multiprocessor computer system clearer. The preamble to claim 1 also addresses these concerns by reciting that the data structure, comprised of the bit masks, is for "storing execution history data indicative of states of threads that are used for providing mutual exclusion between current and next generation data elements." See: Application, pp. 11-15 (definitions and explanations of terms).

Claims 2-6: The Examiner did not specify any missing interrelationships in claims 2 and 3. MPEP § 706.03(d) ¶ 7.34.14, Examiner Note 2. Moreover, claims 2 and 3 do not appear to have any of the interrelationship problems that the Examiner identified in claim 1. Claims 4-6 were only rejected as dependent on claim 3. It is respectfully submitted that all claims are in allowable form.

Response to Section 103 Rejections

Claims 1-6 were rejected under § 103 as unpatentable over the Slingwine reference in view of the Roche reference. [Office Action, p. 4]. Applicant respectfully disagrees.

Claim 1: The Slingwine and Roche references, even as combined by the Examiner, fail to teach or suggest all the limitations of claim 1. As discussed below, the combination suggested by the Examiner fails to encompass first and second level bits masks comprising a data structure,

as recited in claim 1 [See: Office Action, p. 5]. The suggested combination therefore does not contain all the elements of claim 1.

Slingwine is a predecessor to the invention claimed in the current application. The application notes that the Slingwine mechanism (citing U.S.P.N. 5,442,758, the ultimate parent of the Slingwine patent cited by the Examiner) is "not as fast as desired" when applied to certain systems, including systems with non-uniform memory access architecture. [Application, p. 9: 8-10]. An objective of the current invention was therefore "to provide an improved mutual-exclusion mechanism that is less complex and faster than previous mechanisms." [p. 9: 11-12].

The combination of Slingwine and Roche fails to teach or suggest, on a multi-processor computer system with "multiple interconnected processing nodes", a data structure as recited in claim 1 with a "first level bit mask" for node data and "second level bit mask[s]" for processors-within-a-node data. The claim is to the recited data structure in a multiple node computer system, not merely to the use of bit masks to indicate whether a processor or processors have passed through a quiescent state.

The current invention, with data structures such as claim 1's data structure, with first and second level bit masks, in a multi-node computer system is much faster than Slingwine:

> "A high-speed method for maintaining a summary of thread activity reduces the number of remote-memory operations for an n processor, multiple node computer system from n^2 to (2n-1) operations. The method uses a hierarchical summary-of-thread-activity data structure such as first and second level bit masks." [Application, p. 9: 15-19].

The speed advantage described above is huge. For 100 processors, the number of remote-memory operations is reduced from 10,000 to a mere 199. Neither Slingwine nor Roche, either separately or combined as suggested by the Examiner, teaches or suggests claim 1's recited data structure with first and second level bit masks. MPEP § 2143.03.

Nor would there be any motivation to combine the references as suggested by the Examiner. As discussed above, the data structure recited in claim 1 is not shown by the primary reference, Slingwine. The secondary reference, Roche, is completely unrelated and recites partitioned clock stopping in response to processor errors. The references are clearly unrelated and applicant respectfully requests the Examiner to point to where any motivation to combine

these two disparate references can be found. MPEP §§ 706.02(j) and 2143.01. Applicant believes no motivation to combine exists.

Claim 2-6: The Examiner did not demonstrate any reasoning for finding claims 2 or 3 obvious and they are not obvious. These claims are not rendered prima facie obvious. Because, as argued above, claims 1-3 are not obvious, neither are dependent claims 4-6. MPEP § 2143.03. All claims are patentable over Slingwine and Roche.

Conclusion

For the reasons stated the rejections under § 112, 2nd Paragraph, and § 103 should be reconsidered and withdrawn. Further, because no prima facie case of obviousness was established against any claim, if there is a further rejection, it should not be final. Applicant believes the claims are in condition for allowance and requests the Examiner to issue a Notice of Allowance.

Respectfully submitted,

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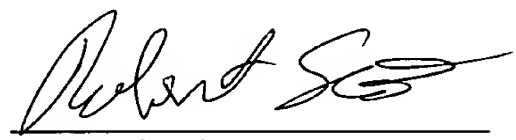
By 

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Marked-up Version of Amended Claims
Pursuant to 37 C.F.R. §§ 1.121(b)-(c)

1. (Amended) In a multiprocessor computer system having multiple interconnected processing nodes each with one or more processors and physical memory, a data structure for storing execution history data indicative of states of threads that are used for providing mutual exclusion between current and next generation data elements, comprising:

a first level bit mask stored in physical memory accessible to all nodes and containing a bit per node, the bit indicating whether the corresponding node contains a processor that has not yet passed through a quiescent state; and

a second level bit mask stored in the physical memory of each processing node and containing a bit per processor associated with a particular node identified in the first level bit mask, the bit indicating whether the corresponding processor has not yet passed through a quiescent state.